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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,913	04/10/2001	A. Nicholas Sporck	P136-US	5250

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,913	SPORCK ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 42 is objected to because of the following informalities: in the amending claim 42, last line, the phrase "an electric circuit" should be changed to --the electric circuit-- to avoid a duplicant positive recitation of the phrase in the claim. Furthermore, the addition of the last line seems to already be claim in line 6 that states "...daughter card means for physically supporting at least a portion of an electric circuit..." Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 19-25, 37-39, 42, 45-50 and 55-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Khoury et al (6232669).

Regarding claim 1, Khoury et al disclose [see Fig. 9] a probe card assembly (interface assembly 140 shown in Fig. 2) for electrically communicating test data between a semiconductor test apparatus (test head 100 of Fig. 2) and a semiconductor device under test (wafer 300), the probe card assembly comprising a substrate (20) con figured to electrically contact the semiconductor tester apparatus (100), a plurality of probes (contactors 30) configured to electrically contact the semiconductor device under test (300), the plurality of probes (30)

located to a first side [referring to bottom side] of the substrate (20) and a daughter card (routing board 260) located to a second side [referring to top side] of the substrate (20) wherein the daughter card (260) being substantially coplanar to the substrate (20), there being a space [via conductive elastomer 250] between the daughter card (260) and the substrate (20).

Regarding claim 2, Khoury et al disclose an electric circuit (interconnect traces 263) is disposed on the daughter card (260).

Regarding claim 3, Khoury et al disclose the electric circuit (263) includes active circuit elements.

Regarding claim 4, Khoury et al disclose the electric circuit (263) is configured to enhance test capabilities of the semiconductor test apparatus (100).

Regarding claim 5, Khoury et al disclose the electric circuit (263) is configured to customize at least portion of the test data to test needs of said semiconductor device under test (300).

Regarding claim 6, Khoury et al disclose the test data comprises test signals generated by said semiconductor test apparatus (100) and the electric circuit (263) customizes at least portion of the test signals [see Abstract].

Regarding claim 7, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (263) customizes at least portion of the response signals [see col. 8, line 40 - col. 9, line 13].

Regarding claim 19, Khoury et al disclose [see Fig. 9] a method of making a probe card assembly (interface assembly 140 shown in Fig. 2), the method comprising providing a substrate (20) including a plurality of tester contacts (contacts 31), disposing a plurality of probes

(contactors 30) to a first side [referring to bottom side] of the substrate (20) and configured to electrically contact a semiconductor device under test (wafer 300), and disposing a daughter card (routing board 260) to a second side [top side] of the substrate (20) wherein the daughter card (260) being substantially coplanar to the substrate(102), there being a space [via conductive elastomer 250] between the daughter card (260) and the substrate (20).

Regarding claim 20, Khoury et al disclose providing an electric circuit (interconnect traces 263) and disposing the electric circuit (263) on the daughter card (20).

Regarding claim 21, Khoury et al disclose the electric circuit (263) includes active circuit elements.

Regarding claim 22, Khoury et al disclose the electric circuit (263) is configured to enhance test capabilities of the semiconductor test apparatus (300) [see Abstract].

Regarding claim 23, Khoury et al disclose the electric circuit (263) is configured to customize test data to test needs of said semiconductor device under test (300).

Regarding claim 24, Khoury et al disclose the test data comprises test signals to be input into the semiconductor device under test (300) and the electric circuit (263) customizes at least portion of the test signals.

Regarding claim 25, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (263) customizes at least portion of the response signals.

Regarding claims 37-39, Khoury et al disclose the probe card assembly (100) made using the process of claims 19-20 and 22.

[Note: "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)]

Regarding claim 42, Khoury et al disclose [see Fig. 9] a probe card assembly (interface assmebly140 shown in Fig. 2) comprising a printed circuit means (substrate 20) for electrically communicating with a semiconductor tester apparatus (test head100), contact means (contactors 30) configured to electrically communicating with semiconductor device under test (300), the contact means (30) being secured to a first side [bottom side] of the printed circuit means (20) and daughter card means (routing board 260) for physically supporting at least portion of an electric circuit (interconnect traces 263), the daughter card means (260) secured to a second side [top side] of the printed circuit means (20) wherein the daughter card (260) being substantially coplanar to the printed circuit means (20).

Regarding claim 45, Khoury et al disclose the electric circuit (263) includes processing means for processing test data for testing the semiconductor device under test (300).

Regarding claim 46, Khoury et al disclose the processing means (263) enhances test capabilities of the semiconductor test apparatus (100).

Regarding claim 47, Khoury et al disclose the processing means (263) customizes the test data to meet test needs of said semiconductor device under test (300).

Regarding claim 48, Khoury et al disclose the test data comprises test signals to be input into the semiconductor device under test (300) and the processing means (263) customizes at least portion of the test signals.

Regarding claim 49, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the processing means (263) customizes at least portion of the response signals.

Regarding claim 50, Khoury et al disclose [see Fig. 9] a probe card assembly (interface assembly 140 shown in Fig. 2) for electrically communicating test data between a semiconductor test apparatus (test head100 shown in Fig. 2) and a semiconductor device under test (wafer 300), the probe card assembly comprising a printed circuit board (substrate 20) con figured to electrically contact the semiconductor tester apparatus (100), a plurality of probes (contactors 30) configured to electrically contact the semiconductor device under test (300), a daughter card (routing board 260) secured to the printed circuit board (30) [via conductive elastomer 250] wherein the daughter card (1260) being substantially coplanar to the printed circuit board (20) and an electric circuit (interconnect traces 263) enhances test capabilities of the semiconductor test apparatus (100) and is disposed on the daughter card (260).

Regarding claim 55, Khoury et al disclose the electric circuit (263) enhances test capabilities of the semiconductor test apparatus (100) by processing at least portion of the test data.

Regarding claim 56, Khoury et al disclose the test data comprises test signals generated by the semiconductor tester apparatus (100) and the electric circuit (263) processes at least portion of the test signals.

Regarding claim 57, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (263) processes at least portion of the response signals.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 8-18, 26-36, 40-41, 43-44 and 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Khoury et al (6232669).

Regarding claims 8-9, 16, 18, 26-27, 34, 36, and 51-55, Khoury et al disclose a daughter card (routing board 260) located to a second side [referring to top side] of the substrate (20) wherein the daughter card (260) being substantially coplanar to the substrate (20). However, they do not disclose a plurality of daughter cards as claimed. It is well known to have more than one daughter card where needed (see MPEP 2144.04 *In re Harza*, 274 F.2d 669, 124 USPQ 378

(CCPA 1960)). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have more than one daughter card since the plurality of cards, which is mere duplication of a single daughter card, would provide support to selective manner to each individual user that will like to duplicate the function of processing signals passing between a semiconductor tester and a semiconductor device under test.

Regarding claims 10, 17, 28, and 35, Khoury et al disclose an electric circuit (interconnect traces 263) is disposed on the daughter card (260).

Regarding claims 11, 29, Khoury et al disclose the electric circuit (263) includes active circuit elements.

Regarding claims 12, 30, Khoury et al disclose the electric circuit (263) is configured to enhance test capabilities of the semiconductor test apparatus (test head100) [see Abstract].

Regarding claims 13, 31, Khoury et al disclose the electric circuit (263) is configured to customize at least portion of the test data to test needs of said semiconductor device under test (300).

Regarding claims 14, 32, Khoury et al disclose the test data comprises test signals generated by said semiconductor test apparatus (100) and the electric circuit (263) customizes at least portion of the test signals.

Regarding claims 15, 33, Khoury et al disclose the test data comprises response signals generated by said semiconductor device under test (300) and the electric circuit (263) customizes at least portion of the response signals.

Regarding claims 40-41, Khoury et al disclose the probe card assembly (100) made using the process of claims 26 and 30.

[Note: "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)]

Conclusion

7. Applicant's arguments with respect to claims 1-57 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (703) 305-1653. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
September 10, 2003

VINH P. NGUYEN
PRIMARY EXAMINER
GROUP 2829
09/12/03